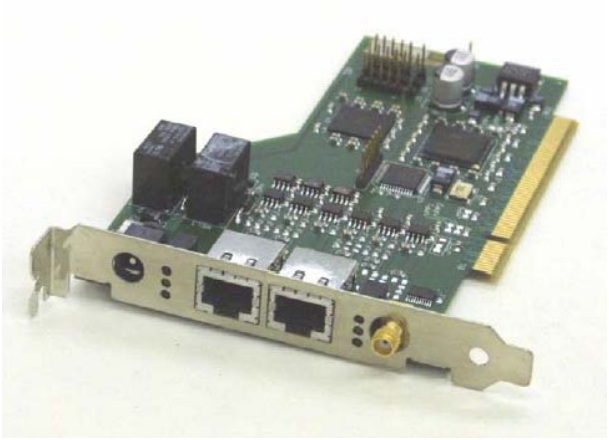
Network Interface Controller

MODEL 6100

- **Supports IntelliBus Protocol**
- **66Mhz, 32bit 3.3V PCI v2.2 Card**
- **Two IntelliBus Serial Ports**
- **Full and Half Duplex Support**
- **RS-485 Physical Layer**
- **Synchronous Data Rates up to 15 Mbps**
- **Asynchronous Data Rates of 1.2 Kbps to 10 Mbps**
- **1K Words Deep Receiver FIFOs**
- **External IntelliBus Power Source**

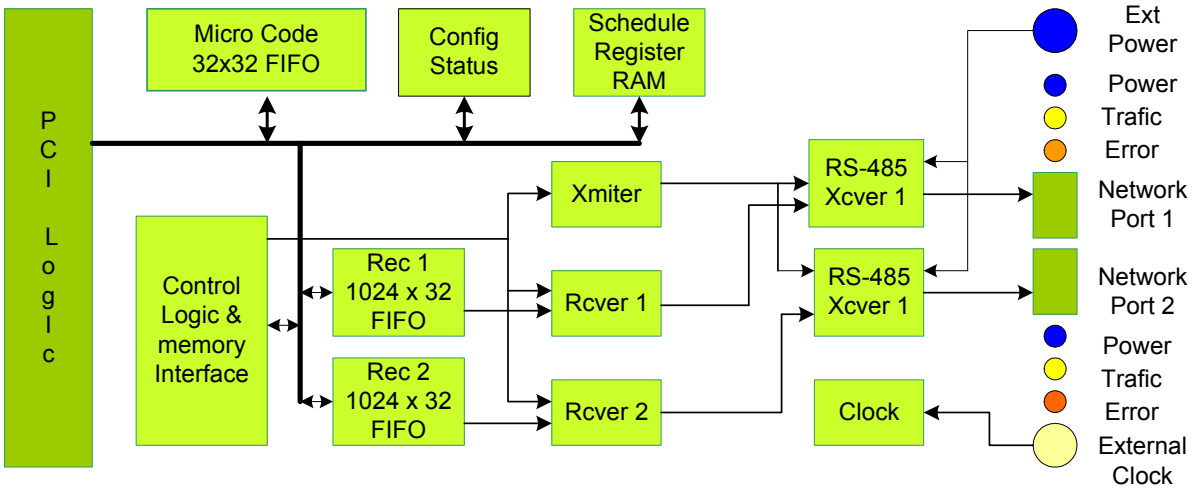


Description

The **VIP Sensors Model 6100 Network Interface Controller (NIC)** card plugs directly into a 66Mhz, 32 bit 3.3V PCI V2.2 compliant slot in a PC compatible computer. The card supports two IntelliBus serial network channels, with isochronous data rates of up to 15Mbps. The IntelliBus network physical layer is RS485 configured as a Half Duplex arrangement.

The Model 6100 card contains a 1K word deep FIFO for each of the two network receiver channels. This allows real time data collection using a standard PC operating system. All control and data retrieval operations are handled by software thru registers implemented in the PCI interface. The card supports a custom microcode instruction set that is used to control the execution of a schedule. The microcode is loaded, by software, into onboard schedule memory.

The NIC card is form factor compatible with normal 3.3 Volt PCI cards. The faceplate provides IntelliBus network connections, run and fault indicators, IntelliBus power connection, and external clock connection.



Network Interface Controller (NIC) Functional Diagram

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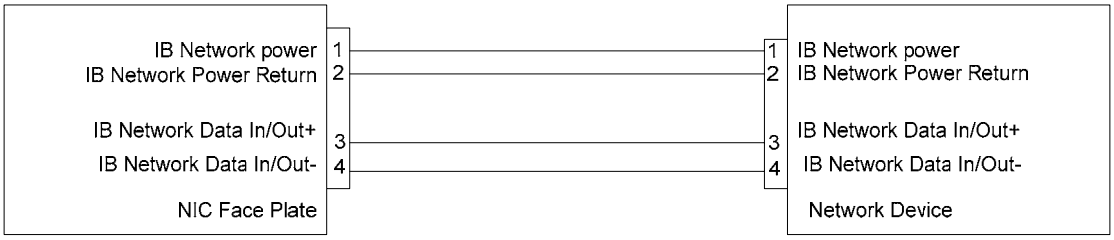
IntelliBus Network Interface

Both channels share the same transmitter logic but have independent receivers. This means that only one IntelliBus schedule can be executed at a time, however, data can be directed to either channel 1, 2 or both. The intent of the second channel is to provide a redundant bus, which can be used for fault tolerance. Both channels support an RS485 physical layer and are configured for Half Duplex isochronous operation. Half Duplex operation implies the IntelliBus messages from the NIC and responses from the network devices share the same wire pair and thus require only two wires for data transmission. This mode results in the fewest number of wires required for the network.



IntelliBus Power (External Power)

The NIC provides power to the devices attached to the IntelliBus network. This power is obtained from an external power source that is connected to the NIC via the External Power jack located on the faceplate of the card.

Schedule Loading/Execution

The order and timing of all IntelliBus network traffic is defined by an IntelliBus schedule. This schedule, created by the user with the assistance of the application Software, is a list of sequentially executed microcode instructions, which dictate the timing and action that is to be performed by the NIC.

There are two methods for schedule execution. The first, which is the primary method, is that the host computer loads the schedule into the NIC's onboard SRAM. It then sets the Microcode Source and Run Microcode bits in the NIC Interface Control register and execution of the schedule begins. Once the schedule execution starts it is independent of the host computer. This allows the host computer to spend time on other tasks such as data processing. This also insures a time deterministic execution of the schedule based strictly on the accuracy of the NIC's onboard oscillator.

The second method for schedule execution is that the host computer feeds the schedule into the NIC's Microcode FIFO. There is no schedule address in this method, hence, the order in which the schedule is executed depends on the order in which the FIFO was filled. This means the host computer needs to continually fill the Microcode FIFO. With this method the NIC cannot insure time deterministic execution of the schedule. The advantage of this second method is that it allows the host computer to execute a second schedule (i.e. send IntelliBus messages) loaded in SRAM. This is

useful for doing temporary operations that are not a part of the regular schedule, such as obtaining status or memory programming operations.

Schedule Registers
Schedule registers are used to simplify the task of dynamically changing the schedule. This is most commonly used in control applications where the data being sent to the IntelliBus network (more specifically network actuator devices) is calculated by the host computer. The schedule registers are also used to provide dynamic data to microcode instructions that perform internal NIC functions such as delays or jumps.

Transmitter
The NIC contains one transmitter, which drives both IntelliBus network channels simultaneously. Each channel can be enabled independently. The data to be transmitted as well as the type of data is provided by the schedule execution logic. There are two types of data or IntelliBus words, Command Words and Data/Argument Words. The transmitter first takes the raw data and formats it into a proper IntelliBus Word. This is done by calculating and adding a parity bit at the end of the word and adding the appropriate sync pattern at the beginning of the word. The transmitter then serializes the data and passes it to the RS485 transceivers. The rate at which the transmitter operates is dependent on the clock selection setting and the bit rate divisor setting.

Receiver
The NIC contains two independent asynchronous receivers. Each receiver has a dedicated FIFO, which is used to accumulate the received data. Once data has been received the FIFO generates an interrupt to notify the host computer that data is available. The host computer can then access the data thru the PCI interface. The receiver detects the start of an IntelliBus word by looking for a valid sync pattern. There are two types of IntelliBus words, Command Words and Data/Argument Words. Each word is preceded by a unique sync pattern. Once a valid sync pattern has been detected the receiver locks itself to the pattern and begins receiving the data bits. The data bits are encoded using a Manchester (or bi-phase) encoding scheme, which means each bit contains a transition. In order to maximize the receiver's tolerance to bit deviations, the receiver relocks itself to each bi-phase transition and repositions for receiving the next data bit. The receiver also monitors the integrity of the received words by checking for bi-phase and parity errors. The receiver calculates the parity and compares the results against the parity bit contained in the word. If the parity matches, word is flagged as valid, otherwise it is flagged as invalid. A bi-phase error occurs when the expected transition is missing in the data bit. When a missing transition is detected, the received processes is aborted and an invalid word with additional bits indicating a bi-phase error are passed to the receiver FIFO.

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SPECIFICATIONS

The following performance specifications are at +75°F (+24°C), unless otherwise noted.

General Specifications

Protocol	IntelliBus v1.0
PCI Bus Interface	66Mhz, 32bit, 3.3V, PCI v2.2
Asynchronous Bit Rates	1.2K to 10 Mbps (binary steps)
Synchronous Bit Rates	Up to 15 Mbps
Receiver FIFO size	1024 Words
MicroCode FIFO size	32 Words
Schedule Register size	256K Words
Schedule Memory size	256K Words

Electrical Characteristics	**Units**	**Min**	**Typical**	**Max**	**Comments**
IntelliBus Network Interface					
IB Network Data & Clock					
Differential Output Voltage	V	1.5		5.0	R = 27 Ω
Common-Mode Output Voltage	V			3.0	R = 27 Ω or 50 Ω
Output Short Circuit Current	mA	35.0		250	-7 V ≤ Vo ≤ +12 V
Differential Input Threshold Voltage	V	-0.2		0.2	-7 V ≤ Vcm ≤ +12 V
Input Resistance	kΩ	12.0			-7 V ≤ Vcm ≤ +12 V
Input Current	mA			1.0	Vin = 12 V
Input Voltage Hysteresis	mV		70.0		Vcm = 0 V
IB Network Power Voltage (1)	V		14	100	
IB Network Power Current (1)	A		3.0		
External Signal Interface					
Ext. Bus Power Voltage (2)			14	100	
Ext. Bus Power Current	A			3.0	
Ext. Clock High Level Input Voltage	V	2.0			
Ext. Clock Low Level Input Voltage	V		0.8		

Note 1: This is the maximum limit allowed by the NIC circuitry; the realistic limitation is set by the selected external supply.
Note 2: This is the maximum limit allowed by the NIC circuitry; the realistic limitation is set by the selected Network devices.